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09/748,165	12/27/2000	Nigel C. Paver	ITL.2094US (P9855)	5048

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
05/19/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/748,165	PAVER, NIGEL C.	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-9,11-14,16 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-9,11-14,16 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/30/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-4, 6-9, 11-14, 16, and 23-25 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Power of Attorney as received on 3/6/2009, RCE and Amendment as received on 3/18/2009, and IDS as received on 3/30/2009.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The disclosure is objected to because of the following informalities:

- On page 8, line 1, please correct the phrase "Fig.3 is an of an example…".

Appropriate correction is required.

Claim Objections

5. Claims 7 and 12 are objected to because of the following informalities: Please replace "represent" with --represents--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Referring to claim 1:

- In the paragraph beginning with "a status register…", it is unclear whether applicant intends for each set of arithmetic flags to have M bits or if one of a plurality of data items has M bits. Applicant should reword this paragraph such that it is clear.
- It is not clear what the arithmetic flags represent with respect to a plurality of data items. That is, applicant claims that each set of arithmetic flags is associated with one of a plurality of data items (1st paragraph of the body of claim 1) wherein the plurality of arithmetic flags represent a result status of the plurality of data items after a mathematical operation is performed by a processor on the plurality of data items (3rd paragraph of the body of the claim). It is not clear if applicant is equating a data item to a result of a mathematical operation or an operand of a mathematical operation. If interpreted as a result, is a mathematical operation really performed on the result, as claimed? The examiner asserts that a mathematical operation is generally performed on operands (not on a result) in order to achieve a result. However, if the data item is interpreted as an operand, do the arithmetic flags really represent a result status of the operands? The examiner asserts that the arithmetic flags represent a

result status of results of mathematical operations performed on operands, not the status of the operands themselves. Applicant should clarify the claim.

9. Referring to claim 7, it is not clear what the arithmetic flags represent with respect to a plurality of data items. That is, it is not clear if applicant is equating a data item to a result of a mathematical operation or an operand of a mathematical operation. If interpreted as a result, is a mathematical operation really performed on the result, as claimed? The examiner asserts that a mathematical operation is generally performed on operands (not on a result) in order to achieve a result. However, if the data item is interpreted as an operand, do the arithmetic flags really represent a result status of the operands? The examiner asserts that the arithmetic flags represent a result status of results of mathematical operations performed on operands, not the status of the operands themselves. Applicant should clarify the claim.

10. Referring to claim 12:

- The preamble sets forth an apparatus, but applicant claims method steps. Hence, applicant should either change the claim to a method claim or insert language to make the claim a hardware apparatus.
- It is not clear what the arithmetic flags represent with respect to a plurality of data items. That is, it is not clear if applicant is equating a data item to a result of a mathematical operation or an operand of a mathematical operation. If interpreted as a result, is a mathematical operation really performed on the result, as claimed? The examiner asserts that a mathematical operation is generally performed on operands (not on a result) in order to achieve a result. However, if the data item is interpreted as an operand, do the arithmetic flags really represent a result status of

the operands? The examiner asserts that the arithmetic flags represent a result status of results of mathematical operations performed on operands, not the status of the operands themselves. Applicant should clarify the claim.

11. Referring to claim 23:

- In the paragraph beginning with "a processor having…", it is unclear whether applicant intends for each set of arithmetic flags to have M bits or if one of a plurality of data items has M bits. Applicant should reword this paragraph such that it is clear.
- It is not clear what the arithmetic flags represent with respect to a plurality of data items. That is, it is not clear if applicant is equating a data item to a result of a mathematical operation or an operand of a mathematical operation. If interpreted as a result, is a mathematical operation really performed on the result, as claimed? The examiner asserts that a mathematical operation is generally performed on operands (not on a result) in order to achieve a result. However, if the data item is interpreted as an operand, do the arithmetic flags really represent a result status of the operands? The examiner asserts that the arithmetic flags represent a result status of results of mathematical operations performed on operands, not the status of the operands themselves. Applicant should clarify the claim.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 3-4, 6-9, 11-14, 16, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golston, U.S. Patent No. 6,026,484.

14. Referring to claim 1, Golston has taught a device comprising:

a) a status register to store a word including a plurality of arithmetic flags, each flag associated with one of a plurality of data items of varying field sizes. See Fig.5, status register 211, and column 21, line 56, to column 22, line 17.

b) a combination function module to examine the word stored in the status register to determine a data item field size for the word (see Table 4 in column 22, and note that size must be determined to determine which bits to combine), and based on the determination of the data item field size to logically combine the plurality of arithmetic flags within the word into a single combined arithmetic flag variable, and to store the single combined arithmetic flag variable into a second register (see Fig.5, register 210, and column 19, lines 1-46), wherein in combining, the combination function module performs an OR operation (see column 19, lines 14-22).

c) wherein the plurality of arithmetic flags represent a result status of the plurality of data items after a mathematical operation is performed by a processor on the plurality of data items. Essentially, an arithmetic operation may be performed on multiple data items at once. For instance, if there are four data items to operate on, then four arithmetic flags will be set in

register 211 (Fig.5). Then, the arithmetic flags are combined into one flag (via OR operation) and the combined result is stored in the appropriate flag section of register 210 (Fig.5 and Fig.6).

d) a condition check module to determine the result status of the combined arithmetic flag variable and cause the processor to execute an appropriate operation based on the result status. See column 5, lines 39-40. Note that the status bits are checked to control conditional execution, as is known in the art.

e) Golston has not taught storing a word including a plurality of sets of arithmetic flags, each set having M bits, and logically combining the plurality of arithmetic flags of the sets within the word into a single combined arithmetic flag variable of M bits. That is, Golston has taught storing just a single flag bit at a time for each data item and combining each data item's flag bit into a single combined arithmetic variable comprising a single bit. See column 21, lines 41-45, Table 4 in column 22, and the examples in columns 77-78. For instance, in Table 4, Golston shows storing four carry bits for four data items, and then combining those four carry bits into a single, global carry bit (column 19, lines 17-22). However, Golston has taught the general concept of storing multiple status flags in a single register, as is known in the art (see Fig.6, and note that negative (N), carry (C), overflow (V), and zero (Z) bits are generally stored in the same register). In addition, Golston has taught that it is desirable to also store and combine all of the arithmetic flags. See column 19, lines 1-46, column 21, lines 41-45, and column 22, lines 14-17. As a result, in order to indicate more than one status for each data item at a given time, as currently proposed by Golston, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Golston to include a larger status identifier so that multiple status indications could be made for each data item, and multiple global status indications would

be realized after combining the sets of flags. This would allow the system to branch based on different statuses. One that would be willing to trade more hardware for increased status indication functionality would be motivated to make such a modification given that it is already known to store all arithmetic flags at once on a smaller scale (as shown in Fig.6).

15. Referring to claim 3, Golston, as modified, has taught the device recited in claim 1, wherein the field size is based on a nibble, byte, half-word, or word in length. See column 20, Table 2, and lines 38-45).

16. Referring to claim 4, Golston, as modified, has taught the device recited in claim 3, wherein the plurality of arithmetic flags further comprise a negative data value, a zero data value, a carry out occurrence in a data value, or an overflow condition in a data item in the plurality of data items. See Fig.6 and column 19, lines 1-46.

17. Referring to claim 6, Golston, as modified, has taught the device recited in claim 1, wherein the result status determined by the condition further comprises:

a) any data item has overflowed. See column 19, lines 23-37, and note that if the V bit set, overflow is detected.

b) any data item has not overflowed. See column 19, lines 23-37, and note that if the V bit is clear, overflow is not detected.

c) any data item is positive or zero. See column 19, lines 1-13, and note that if the N bit is clear, a positive or zero data item is detected.

d) any data item is negative. See column 19, lines 1-13, and note that if the N bit is set, a positive or zero data item is detected.

e) any data item is zero. See column 19, lines 38-46, and note that if the Z bit is set, a zero data item is detected.

f) any data item is not zero. See column 19, lines 38-46, and note that if the Z bit is clear, a zero data item is detected.

g) any data item has a carry out. See column 19, lines 14-22, and note that if the C bit is set, a carry is detected.

h) any data item does not have a carry out. See column 19, lines 14-22, and note that if the C bit is clear, a carry is not detected.

i) all data items have overflowed. See column 19, lines 23-37, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so overflow of all data items can be checked.

j) all data items have not overflowed. See column 19, lines 23-37, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so non-overflow of all data items can be checked.

k) all data items are positive or zero. See column 19, lines 1-13, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are zero or positive.

l) all data items are negative. See column 19, lines 1-13, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so negativity of all data items can be checked.

m) all data items are zero. See column 19, lines 38-46, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are zero.

n) all data items are not zero. See column 19, lines 38-46, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are non-zero.

o) all data items have a carry out. See column 19, lines 14-22, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so carry out of all data items can be checked.

p) all data items do not have a carry out. See column 19, lines 14-22, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so non-carry out of all data items can be checked.

18. Referring to claim 7, Golston has taught a method comprising:

a) determining a field size of a plurality of arithmetic flags stored in a status register of a processor on which to base a combination process, wherein the plurality of arithmetic flags represent a result status of a plurality of data items after a mathematical operation is performed by the processor on the plurality of data items. See column 19, lines 1-46, column 20, lines 46-50, column 21, lines 56-67, and Table 4 in column 22.

b) extracting the plurality of arithmetic flags from the status register based on the field size and logically combining the plurality of arithmetic flags based on a function selected when a combination process is selected, wherein the function comprises an OR operation. See column 19, lines 14-22.

d) storing a result of the combining of the plurality of arithmetic flags in a destination register for access by the processor. See column 19, lines 14-22. Essentially, an arithmetic operation may be performed on multiple data items at once. For instance, if there are four data items to operate on, then four arithmetic flags will be set in register 211 (Fig.5). Then, the four arithmetic flags

are combined into one flag (via OR operation) and the combined flag is stored in the appropriate flag section of register 210 (Fig.5 and Fig.6).

e) Golston has not taught that the status register stores a plurality of sets of arithmetic flags, wherein each set of flags represents a result status of a data item of the plurality of data, extracting the plurality of sets of flags, and logically combining the plurality of sets of arithmetic flags. That is, Golston has taught storing just a single flag bit at a time for each data item and combining each data item's flag bit into a single combined arithmetic variable comprising a single bit. See column 21, lines 41-45, Table 4 in column 22, and the examples in columns 77-78. For instance, in Table 4, Golston shows storing four carry bits for four data items, and then combining those four carry bits into a single, global carry bit (column 19, lines 17-22). However, Golston has taught the general concept of storing multiple status flags in a single register, as is known in the art (see Fig.6, and note that negative (N), carry (C), overflow (V), and zero (Z) bits are generally stored in the same register). In addition, Golston has taught that it is desirable to also store and combine all of the arithmetic flags. See column 19, lines 1-46, column 21, lines 41-45, and column 22, lines 14-17. As a result, in order to indicate more than one status for each data item at a given time, as currently proposed by Golston, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Golston to include a larger status identifier so that multiple status indications could be made for each data item, and multiple global status indications would be realized after combining the sets of flags. This would allow the system to branch based on different statuses. One that would be willing to trade more hardware for increased status indication functionality would be motivated to make

such a modification given that it is already known to store all arithmetic flags at once on a smaller scale (as shown in Fig.6).

19. Referring to claim 8, Golston, as modified, has taught a method as described in claim 7. Furthermore, claim 8 is rejected for the same reasons set forth in the rejection of claim 3.

20. Referring to claim 9, Golston, as modified, has taught a method as described in claim 8. Furthermore, claim 9 is rejected for the same reasons set forth in the rejection of claim 4.

21. Referring to claim 11, Golston, as modified, has taught a method as described in claim 7. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 6.

22. Referring to claim 12, claim 12 is rejected for the same reasons set forth in the rejection of claim 7.

23. Referring to claim 13, Golston, as modified, has taught an apparatus as described in claim 12. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 3.

24. Referring to claim 14, Golston, as modified, has taught an apparatus as described in claim 13. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 4.

25. Referring to claim 16, Golston, as modified, has taught an apparatus as described in claim 12. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 6.

26. Referring to claim 23, claim 23 is rejected for the same reasons set forth in the rejection of claim 1.

27. Referring to claim 24, Golston, as modified, has taught the system of claim 23, wherein the processor includes at least three stages of pipelining. See Fig.4.

28. Referring to claim 25, Golston, as modified, has taught the system of claim 24, wherein the at least three stages of pipelining include a fetch stage, a decode stage, and an execute stage.

See Fig.4, and note the fetch and execute stages. In between is a decode stage, which accepts fetched instructions, decodes them, and sends the execution unit the appropriate signals. See Fig.5, component 250.

Response to Arguments

29. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Auslander et al., U.S. Patent No. 4,589,087, has taught producing carry flags for N parallel operations, and then combining the N flags into a single global carry flag which is stored in a CD filed of a register (Fig.3).

Thekkath et al., U.S. Patent No. 6,714,197, has taught combining condition code bits so that branch occurs based on a specified combination of condition codes as opposed to any one condition code.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
April 15, 2009